PROPRIETARY NOTICE

VME64 SVEC

Simple VME FMC Carrier

(hardware manual)

Version 1.1

preliminary

refers to product revision no.
V 2.0

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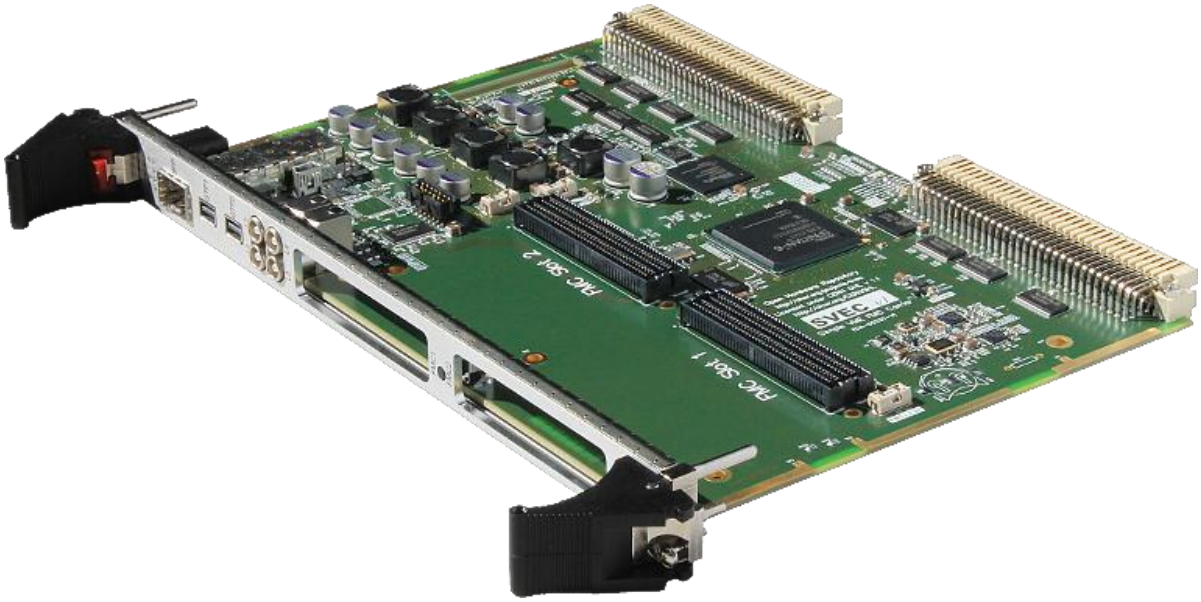


Im Doerener Feld 8
33100 Paderborn, Germany

Tel.:	+49-5251-1550-0
FAX:	+49-5251-1550-190
email:	support@janztec.com
Internet:	www.janztec.com

Contents

List of Figures

List of Tables

About this Manual

This is the hardware manual for the VME64 SVEC computer system. It gives all necessary information to programmers of the VME64 SVEC. We have tried to keep it compact, so there are no special sections for users and programmers. I.e. everything that can be said about the serial port is said in one place (connector layout, signal levels and programming hints). Users that are not programmers might therefore only read the first section (Introduction), and come back to the detailed sections when they need special information.

The manual starts with an **Introduction** to the VME64 SVEC. This is some prose that describes the features and architecture of the VME64 SVEC. You should already know this if you have bought the board!
The rest of the manual then covers **technical details** about the VME64 SVEC.

Conventions

If numbers are specified in this manual, they will be either decimal or hexadecimal. We use C-notation to identify hexadecimal numbers (the 0x prefix).

If we refer to low active signal names, they will suffixed by a "#" character.

Some parts of the text are really important. These are visually marked with the following signs:

Some parts of the manual contain notices you have to observe to ensure your personal safety, or to prevent damage to property. These are visually marked with the following alert symbols:

DANGER

Indicates that death or severe personal injury *will* result if proper precautions are not taken.

WARNING

Indicates that death or severe personal injury *may* result if proper precautions are not taken.

CAUTION

Indicates that *minor* personal injury can result if proper precautions are not taken.

NOTICE

Indicates that damage to equipment can result if proper precautions are not taken.

Indicates information that we think you should have read to save your time by avoiding common problems. Important suggestions that should be followed will also be marked with this sign.

1 Introduction

The Simple VME FMC Carrier (abbr.: SVEC) is a VME64 add in card for VME systems. The functionality is strongly depending on the configuration of the application FPGA which is programmed by the user. The SFPGA is programmed with a bootloader which provides a mechanism to configure the AFPGA via the VME-bus. The SVEC can carry two Mezzanine boards, following the VITA57 standard.

The Carrier-Mezzanine architecture is a modular architecture, so that any kind of specific Mezzanine board can be plugged on the FMC connectors of the SVEC. The SVEC provides FPGA logic, power supplies, memories, clocking resources and interface to the VME bus, while the Mezzanine boards provide application-specific functions.

The design was initiated by CERN and it is an open hardware project [1]. It is licensed under the CERN OHL v1.1 [4]. The Janz Tec AG is a commercial manufacturer for this project

To understand what the open hardware repository is move to the OHWR.

1.1 Order information

Material-No.	Product	Description
BO-FVM-SVEC0	VME64 SVEC	Simple VME FMC Carrier.
KD-FVM-SVEC0	VME64 SVEC	For CERN specific orders.

table 1: SVEC standard product

1.2 Hardware Features

- **VME64x interface**

- **Two Low-Pin Count FMC slots**
  - V_{adj} fixed to 2.5V
  - No dedicated clock signals from Carrier to FMC (as only available on HPC pins and use LPC)
  - FMC connectivity: all 34 differential pairs connected, 1 GTP transceiver with clock, 2 clock pairs, JTAG

- **2 Xilinx FPGAs**
  - **Application** FPGA: Spartan-6 XC6SLX150T-3FGG900C
    - Direct connection to all resources such as VME64x, memories and FMC connectors
  - **System** FPGA: Spartan-6 XC6SLX9-2FTG256C
    - Provides VME bootloader, early oscillator/PLL config
    - Configuration Flash memory for both Main FPGA and Application FPGA configuration

- **FPGA configuration**
  - From SPI flash or via VME

- **Clocking resources**
  - 1x 10-280 MHz I2C Programmable XO Oscillator, starts up at 100 MHz (Silicon Labs Si570, freely usable)
  - 1x 25 MHz TCXO controlled by a DAC with SPI interface (AD5662, used by White Rabbit PTP core)
  - 1x 20 MHz VCXO controlled by a DAC with SPI interface (AD5662, used by White Rabbit PTP core)
  - 2x low-jitter frequency synthesizer/fanout (TI CDCM61004, fixed configuration, Fout=125 MHz, used by White Rabbit PTP core)

- **On-board memories**
  - 2x 256 MByte (2 Gbit) DDR3 (16-bit bus, MT41J128M16HA-15E)
  - 1x 128 Mbit SPI flash for FPGA firmware storage
  - 64kbit EEPROM (24AA64T-I/MC) connected for storing application parameters
  - 1x I2C configuration EEPROM (24LC64)

- **Miscellaneous**
  - On-board thermometer IC (DS18B20U+)
  - Unique 64-bit identifier (DS18B20U+)

- **Front panel**
  - 1x SFP port (White Rabbit compatible)
  - 4x LEMO/SMC programmable I/Os capable of driving 3.3V @ 50 ohm
  - 2x mini DisplayPort connectors for high-speed serial GTP links (not for video)
  - 8x Programmable LED
  - Reset push button

- **Internal connectors**
  - VME P2 connector provides access to a Rear Transition Module (compatible to VFC)
    - 40 user defined single ended (Vcco=2.5V) signals (or 20 LVDS pairs) connected to the Application FPGA
    - 2x 125 MHz LVDS clocks provided to the RTM
  - Xilinx-style JTAG connector

  - Internal mini USB 2.0 High Speed connector for stand-alone applications (CP2103)

- **Optional features**, check with vendor
  - Internal 2 x SATA connector for stand-alone PCI Express connectivity (clock + data)
  - Internal 4 x UFL connectors with low-jitter clock for FMC cards
  - Internal additional USB 2.0 on 4-pin header (FT2232HL)
  - Battery for secure storage of FPGA configuration data
  - Stand-alone features
    - External supply connector (3.3V, 5V) on internal SATA connector
    - PCIe interface on internal SATA connector

2 Safety Instructions

Refer to page 5 for explanation of the warning notice system.

The product described in this documentation may be operated only by personnel qualified for the specific task in accordance with the relevant documentation for the specific task, in particular its warning notices and safety instructions. Qualified personnel are those who, based on their training and experience, are capable of identifying risks and avoiding potential hazards when working with these products.

2.1 Installation and Maintenance

WARNING

The IO interfaces (connectors) of the product are only suited to be connected to SELV circuits.

2.2 Ambient and Environmental Conditions

CAUTION

Do not operate the product beyond the specified ambient conditions. Do not cover the vent slots of the product.

DANGER

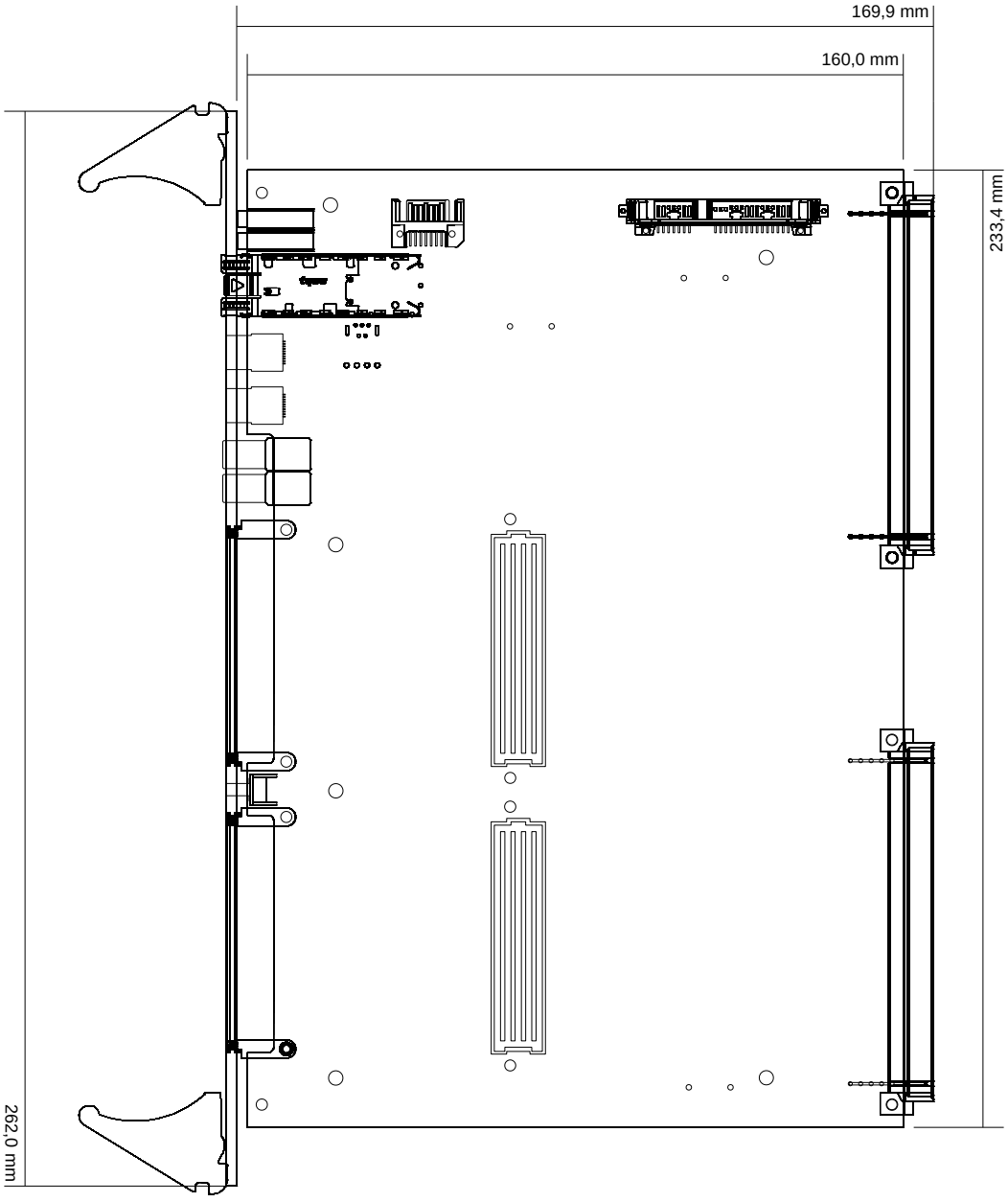
Do not operate this product in potentially explosive atmosphere.

3 Technical overview

When opening the shipping package of the VME64 SVEC, you should immediately check the contents of the package. In the package you will find information about the scope of delivery, as this depends on the options that you have ordered.

The VME64 SVEC is delivered in a properly configured state. That is, CPU and memory are installed.

3.1 Mechanical drawings



3.2 Block diagram

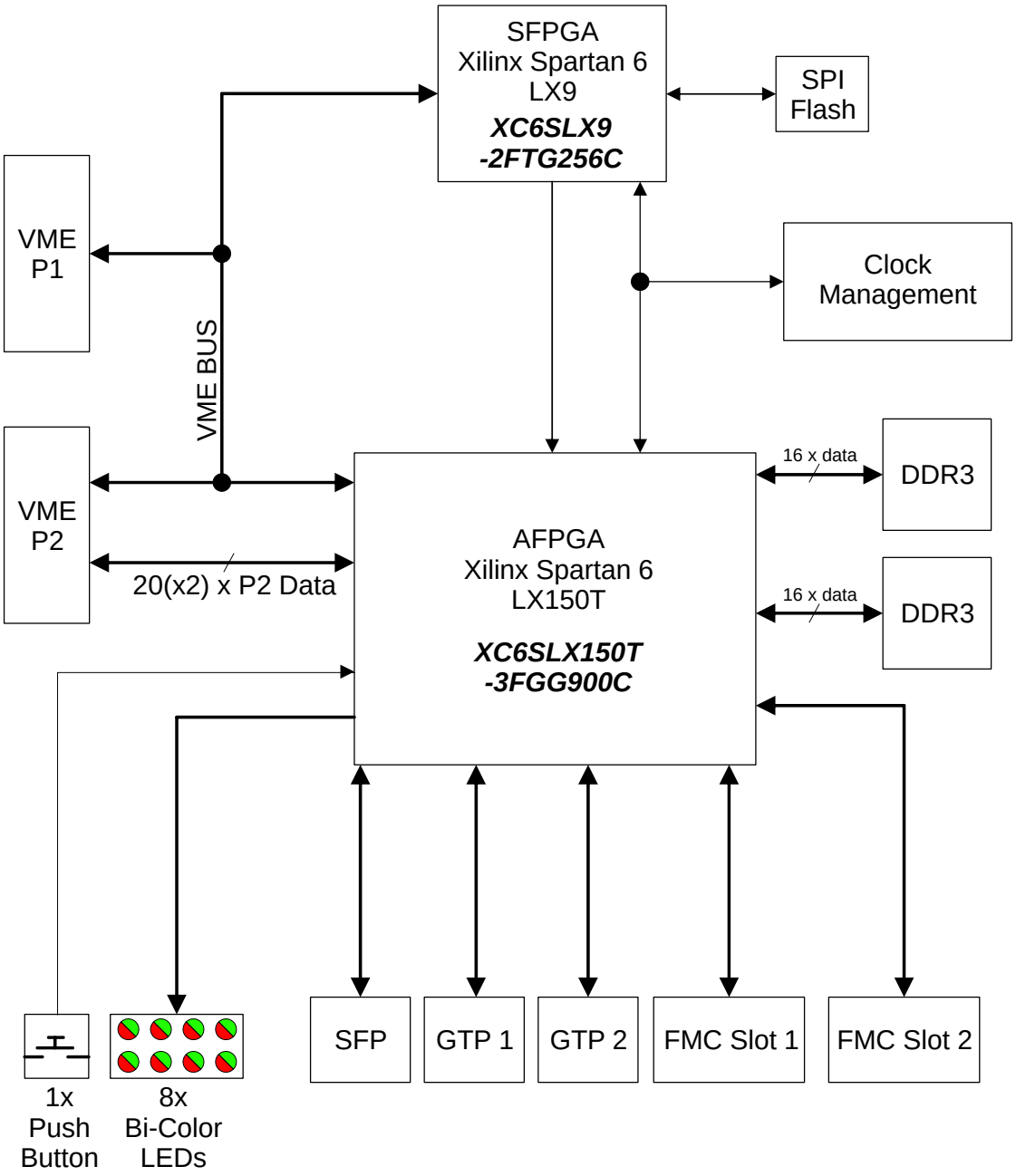


figure 1: block diagram

3.3 FMC Connectors

3.3.1 FMC-Slot 1 - Row C

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	21	GND	-
2	FMC1_DP0C2M_P	fmc1_dp0c2m_p_o	22	FMC1_LA_P18	fmc2_la_p_b[18]
3	FMC1_DP0C2M_N	fmc1_dp0c2m_n_o	23	FMC1_LA_N18	fmc1_la_n_b[18]
4	GND	-	24	GND	-
5	GND	-	25	GND	-
6	FMC1_DP0C2C_P	fmc1_dp0c2c_p_o	26	FMC1_LA_P27	fmc1_la_p_b[27]
7	FMC1_DP0C2C_N	fmc1_dp0c2c_n_o	27	FMC1_LA_N27	fmc1_la_n_b[27]
8	GND	-	28	GND	-
9	GND	-	29	GND	-
10	FMC1_LA_P6	fmc1_la_p_b[6]	30	FMC1_SCL	fmc1_scl_o
11	FMC1_LA_N6	fmc1_la_n_b[6]	31	FMC1_SDA	fmc1_sda_b
12	GND	-	32	GND	-
13	GND	-	33	GND	-
14	FMC1_LA_P10	fmc1_la_p_b[10]	34	FMC_GA0(3V3)	-
15	FMC1_LA_N10	fmc1_la_n_b[10]	35	P12V_FMC1	-
16	GND	-	36	GND	-
17	GND	-	37	P12V_FMC1	-
18	FMC1_LA_P14	fmc1_la_p_b[14]	38	GND	-
19	FMC1_LA_N14	fmc1_la_n_b[14]	39	P3V3_FMC1	-
20	GND	-	40	GND	-

3.3.2 FMC-Slot 1 - Row D

Pin	Signal	UCF	Pin	Signal	UCF
1	FMC1_PFC2M		21	FMC1_LA_N17	fmc1_la_n_b[17]
2	GND	-	22	GND	-
3	GND	-	23	FMC1_LA_P23	fmc1_la_p_b[23]
4	FMC1_GBTCLK0M2C_P	fmc1_gbtclk0m2c_p_i	24	FMC1_LA_N23	fmc1_la_n_b[23]
5	FMC1_GBTCLK0M2C_N	fmc1_gbtclk0m2c_n_i	25	GND	-
6	GND	-	26	FMC1_LA_P26	fmc1_la_p_b[26]
7	GND	-	27	FMC1_LA_N26	fmc1_la_n_b[26]
8	FMC1_LA_P1	fmc1_la_p_b[1]	28	GND	-
9	FMC1_LA_N1	fmc1_la_n_b[1]	29	FMC1_TCK	fmc1_tck_o
10	GND	-	30	FMC1_TDI	fmc1_tdi_i
11	FMC1_LA_P5	fmc1_la_p_b[5]	31	FMC1_TDO	fmc1_tdo_o
12	FMC1_LA_N5	fmc1_la_n_b[5]	32	P3V3_AUX_FMC	-
13	GND	-	33	FMC1_TMS	fmc1_tms_o
14	FMC1_LA_P9	fmc1_la_p_b[9]	34	FMC1_TRST_L	
15	FMC1_LA_N9	fmc1_la_n_b[9]	35	FMC_GA1	GND
16	GND	-	36	P3V3_FMC1	-
17	FMC1_LA_P13	fmc1_la_p_b[13]	37	GND	-
18	FMC1_LA_N13	fmc1_la_n_b[13]	38	P3V3_FMC1	-
19	GND	-	39	GND	-
20	FMC1_LA_P17	fmc1_la_p_b[17]	40	P3V3_FMC1	-

3.3.3 FMC-Slot 1 - Row G

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	21	FMC1_LA_P20	fmc1_la_p_b[20]
2	FMC1_CLK1M2C_P	fmc1_clk1m2c_p_i	22	FMC1_LA_N20	fmc1_la_n_b[20]
3	FMC1_CLK1M2C_N	fmc1_clk1m2c_n_i	23	GND	-
4	GND	-	24	FMC1_LA_P22	fmc1_la_p_b[18]
5	GND	-	25	FMC1_LA_N22	fmc1_la_n_b[18]
6	FMC1_LA_P0	fmc1_la_p_b[0]	26	GND	-
7	FMC1_LA_N0	fmc1_la_n_b[0]	27	FMC1_LA_P25	fmc1_la_p_b[25]
8	GND	-	28	FMC1_LA_N25	fmc1_la_n_b[25]
9	FMC1_LA_P3	fmc1_la_p_b[3]	29	GND	-
10	FMC1_LA_N3	fmc1_la_n_b[3]	30	FMC1_LA_P29	fmc1_la_p_b[29]
11	GND	-	31	FMC1_LA_N29	fmc1_la_n_b[29]
12	FMC1_LA_P8	fmc1_la_p_b[8]	32	GND	-
13	FMC1_LA_N8	fmc1_la_n_b[8]	33	FMC1_LA_P31	fmc1_la_p_b[31]
14	GND	-	34	FMC1_LA_N31	fmc1_la_n_b[31]
15	FMC1_LA_P12	fmc1_la_p_b[12]	35	GND	-
16	FMC1_LA_N12	fmc1_la_n_b[12]	36	FMC1_LA_P33	fmc1_la_p_b[33]
17	GND	-	37	FMC1_LA_N33	fmc1_la_n_b[33]
18	FMC1_LA_P16	fmc1_la_p_b[16]	38	GND	-
19	FMC1_LA_N16	fmc1_la_n_b[16]	39	P2V5_FMC	-
20	GND	-	40	GND	-

3.3.4 FMC-Slot 1 - Row H

Pin	Signal	UCF	Pin	Signal	UCF
1	FMC1_VREFAM2C	-	21	GND	-
2	FMC1_PRSNTM2C_N	-	22	FMC1_LA_P19	fmc1_la_p_b[19]
3	GND	-	23	FMC1_LA_N19	fmc1_la_n_b[19]
4	FMC1_CLK0M2C_P	fmc1_clk0m2c_p_i	24	GND	-
5	FMC1_CLK0M2C_N	fmc1_clk0m2c_n_i	25	FMC1_LA_P21	fmc1_la_p_b[21]
6	GND	-	26	FMC1_LA_N21	fmc1_la_n_b[21]
7	FMC1_LA_P2	fmc1_la_p_b[2]	27	GND	-
8	FMC1_LA_N2	fmc1_la_n_b[2]	28	FMC1_LA_P24	fmc1_la_p_b[24]
9	GND	-	29	FMC1_LA_N24	fmc1_la_n_b[24]
10	FMC1_LA_P4	fmc1_la_p_b[4]	30	GND	-
11	FMC1_LA_N4	fmc1_la_n_b[4]	31	FMC1_LA_P28	fmc1_la_p_b[28]
12	GND	-	32	FMC1_LA_N28	fmc1_la_n_b[28]
13	FMC1_LA_P7	fmc1_la_p_b[7]	33	GND	-
14	FMC1_LA_N7	fmc1_la_n_b[7]	34	FMC1_LA_P30	fmc1_la_p_b[30]
15	GND	-	35	FMC1_LA_N30	fmc1_la_n_b[30]
16	FMC1_LA_P11	fmc1_la_p_b[11]	36	GND	-
17	FMC1_LA_N11	fmc1_la_n_b[11]	37	FMC1_LA_P32	fmc1_la_p_b[32]
18	GND	-	38	FMC1_LA_N32	fmc1_la_n_b[32]
19	FMC1_LA_P15	fmc1_la_p_b[15]	39	GND	-
20	FMC1_LA_N15	fmc1_la_n_b[15]	40	P2V5_FMC	-

3.3.5 FMC-Slot 2 - Row C

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	21	GND	-
2	FMC2_DP0C2M_P	fmc2_dp0c2m_p_o	22	FMC2_LA_P18	fmc2_la_p_b[18]
3	FMC2_DP0C2M_N	fmc2_dp0c2m_n_o	23	FMC2_LA_N18	fmc2_la_n_b[18]
4	GND	-	24	GND	-
5	GND	-	25	GND	-
6	FMC2_DP0C2C_P	fmc2_dp0c2c_p_o	26	FMC2_LA_P27	fmc2_la_p_b[27]
7	FMC2_DP0C2C_N	fmc2_dp0c2c_n_o	27	FMC2_LA_N27	fmc2_la_n_b[27]
8	GND	-	28	GND	-
9	GND	-	29	GND	-
10	FMC2_LA_P6	fmc2_la_p_b[6]	30	FMC2_SCL	fmc1_scl_o
11	FMC2_LA_N6	fmc2_la_n_b[6]	31	FMC2_SDA	fmc1_sda_b
12	GND	-	32	GND	-
13	GND	-	33	GND	-
14	FMC2_LA_P10	fmc2_la_p_b[10]	34	FMC_GA0(3V3)	-
15	FMC2_LA_N10	fmc2_la_n_b[10]	35	P12V_FMC2	-
16	GND	-	36	GND	-
17	GND	-	37	P12V_FMC2	-
18	FMC2_LA_P14	fmc2_la_p_b[14]	38	GND	-
19	FMC2_LA_N14	fmc2_la_n_b[14]	39	P3V3_FMC2	-
20	GND	-	40	GND	-

3.3.6 FMC-Slot 2 - Row D

Pin	Signal	UCF	Pin	Signal	UCF
1	FMC2_PFC2M		21	FMC2_LA_N17	fmc2_la_n_b[17]
2	GND	-	22	GND	-
3	GND	-	23	FMC2_LA_P23	fmc2_la_p_b[23]
4	FMC2_GBTCLK0M2C_P	fmc2_gbtclk0m2c_p_i	24	FMC2_LA_N23	fmc2_la_n_b[23]
5	FMC2_GBTCLK0M2C_N	fmc2_gbtclk0m2c_n_i	25	GND	-
6	GND	-	26	FMC2_LA_P26	fmc2_la_p_b[26]
7	GND	-	27	FMC2_LA_N26	fmc2_la_n_b[26]
8	FMC2_LA_P1	fmc2_la_p_b[1]	28	GND	-
9	FMC2_LA_N1	fmc2_la_n_b[1]	29	FMC2_TCK	fmc2_tck_o
10	GND	-	30	FMC2_TDI	fmc2_tdi_i
11	FMC2_LA_P5	fmc2_la_p_b[5]	31	FMC2_TDO	fmc2_tdo_o
12	FMC2_LA_N5	fmc2_la_n_b[5]	32	P3V3_AUX_FMC	-
13	GND	-	33	FMC2_TMS	fmc2_tms_o
14	FMC2_LA_P9	fmc2_la_p_b[9]	34	FMC2_TRST_L	
15	FMC2_LA_N9	fmc2_la_n_b[9]	35	FMC_GA1	GND
16	GND	-	36	P3V3_FMC2	-
17	FMC2_LA_P13	fmc2_la_p_b[13]	37	GND	-
18	FMC2_LA_N13	fmc2_la_n_b[13]	38	P3V3_FMC2	-
19	GND	-	39	GND	-
20	FMC2_LA_P17	fmc2_la_p_b[17]	40	P3V3_FMC2	-

3.3.7 FMC-Slot 2 - Row G

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	21	FMC2_LA_P20	fmc2_la_p_b[20]
2	FMC2_CLK1M2C_P	fmc1_clk1m2c_p_i	22	FMC2_LA_N20	fmc2_la_n_b[20]
3	FMC2_CLK1M2C_N	fmc1_clk1m2c_n_i	23	GND	-
4	GND	-	24	FMC2_LA_P22	fmc2_la_p_b[18]
5	GND	-	25	FMC2_LA_N22	fmc2_la_n_b[18]
6	FMC2_LA_P0	fmc2_la_p_b[0]	26	GND	-
7	FMC2_LA_N0	fmc2_la_n_b[0]	27	FMC2_LA_P25	fmc2_la_p_b[25]
8	GND	-	28	FMC2_LA_N25	fmc2_la_n_b[25]
9	FMC2_LA_P3	fmc2_la_p_b[3]	29	GND	-
10	FMC2_LA_N3	fmc2_la_n_b[3]	30	FMC2_LA_P29	fmc2_la_p_b[29]
11	GND	-	31	FMC2_LA_N29	fmc2_la_n_b[29]
12	FMC2_LA_P8	fmc2_la_p_b[8]	32	GND	-
13	FMC2_LA_N8	fmc2_la_n_b[8]	33	FMC2_LA_P31	fmc2_la_p_b[31]
14	GND	-	34	FMC2_LA_N31	fmc2_la_n_b[31]
15	FMC2_LA_P12	fmc2_la_p_b[12]	35	GND	-
16	FMC2_LA_N12	fmc2_la_n_b[12]	36	FMC2_LA_P33	fmc2_la_p_b[33]
17	GND	-	37	FMC2_LA_N33	fmc2_la_n_b[33]
18	FMC2_LA_P16	fmc2_la_p_b[16]	38	GND	-
19	FMC2_LA_N16	fmc2_la_n_b[16]	39	P2V5_FMC	-
20	GND	-	40	GND	-

3.3.8 FMC-Slot 2 - Row H

Pin	Signal	UCF	Pin	Signal	UCF
1	FMC2_VREFAM2C	-	21	GND	-
2	FMC2_PRSNTM2C_N	-	22	FMC2_LA_P19	fmc2_la_p_b[19]
3	GND	-	23	FMC2_LA_N19	fmc2_la_n_b[19]
4	FMC2_CLK0M2C_P	fmc1_clk0m2c_p_i	24	GND	-
5	FMC2_CLK0M2C_N	fmc1_clk0m2c_n_i	25	FMC2_LA_P21	fmc2_la_p_b[21]
6	GND	-	26	FMC2_LA_N21	fmc2_la_n_b[21]
7	FMC2_LA_P2	fmc2_la_p_b[2]	27	GND	-
8	FMC2_LA_N2	fmc2_la_n_b[2]	28	FMC2_LA_P24	fmc2_la_p_b[24]
9	GND	-	29	FMC2_LA_N24	fmc2_la_n_b[24]
10	FMC2_LA_P4	fmc2_la_p_b[4]	30	GND	-
11	FMC2_LA_N4	fmc2_la_n_b[4]	31	FMC2_LA_P28	fmc2_la_p_b[28]
12	GND	-	32	FMC2_LA_N28	fmc2_la_n_b[28]
13	FMC2_LA_P7	fmc2_la_p_b[7]	33	GND	-
14	FMC2_LA_N7	fmc2_la_n_b[7]	34	FMC2_LA_P30	fmc2_la_p_b[30]
15	GND	-	35	FMC2_LA_N30	fmc2_la_n_b[30]
16	FMC2_LA_P11	fmc2_la_p_b[11]	36	GND	-
17	FMC2_LA_N11	fmc2_la_n_b[11]	37	FMC2_LA_P32	fmc2_la_p_b[32]
18	GND	-	38	FMC2_LA_N32	fmc2_la_n_b[32]
19	FMC2_LA_P15	fmc2_la_p_b[15]	39	GND	-
20	FMC2_LA_N15	fmc2_la_n_b[15]	40	P2V5_FMC	-

3.4 VME64x Connectors P1 und P2

The VME interface is according to VME64x (VME64 Extensions). VME64x is a superset of VME64 which itself is a superset of the original VMEbus that is specified in IEEE-1014-1987.

The VME Connectors P1 and P2 are connected to both FPGAs (SFPGA and AFPGA). Some signals are connected in special manner; especially the user defined signals. For the detailed connectivity one should consult the SVEC schematic in the Appendix.

Differences at the connector P1:

3.4.1 VME P1 - Row Z

Pin	Signal	UCF	Pin	Signal	UCF
1	VME_TRST	to SFPGA			
3	VME_TCK	to SFPGA			
5	VME_TDO	to SFPGA			
7	VME_TDI	to SFPGA			
9	VME_TMS	to SFPGA			

Differences at the connector P2:

3.4.2 VME P2 - Row A

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	17	P2_DATA_P5	p2_data_p_b[5]
2	P2_DATA_P0	p2_data_p_b[0]	18	P2_DATA_N5	p2_data_n_b[5]
3	P2_DATA_N0	p2_data_n_b[0]	19	GND	-
4	GND	-	20	P2_DATA_P6	p2_data_p_b[6]
5	P2_DATA_P1	p2_data_p_b[1]	21	P2_DATA_N6	p2_data_n_b[6]
6	P2_DATA_N1	p2_data_n_b[1]	22	GND	-
7	GND	-	23	P2_DATA_P7	p2_data_p_b[7]
8	P2_DATA_P2	p2_data_p_b[2]	24	P2_DATA_N7	p2_data_n_b[7]
9	P2_DATA_N2	p2_data_n_b[2]	25	GND	-
10	GND	-	26	P2_DATA_P8	p2_data_p_b[8]
11	P2_DATA_P3	p2_data_p_b[3]	27	P2_DATA_N8	p2_data_n_b[8]
12	P2_DATA_N3	p2_data_n_b[3]	28	GND	-
13	GND	-	29	P2_DATA_P9	p2_data_p_b[9]
14	P2_DATA_P4	p2_data_p_b[4]	30	P2_DATA_N9	p2_data_n_b[9]
15	P2_DATA_N4	p2_data_n_b[4]	31	GND	-
16	GND	-	32	-	-

3.4.3 VME P2 - Row C

Pin	Signal	UCF	Pin	Signal	UCF
23	GND	to SFPGA	28	GND	
24	GND	to SFPGA	29	P2_PLLFMC1_CLK_P	
25	P2_PLLFMC1_CLK_P	to SFPGA	30	P2_PLLFMC1_CLK_N	
26	P2_PLLFMC1_CLK_N	to SFPGA	31	GND	
27	GND	to SFPGA	32	GND	

3.4.4 VME P2 - Row D

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	17	P2_DATA_P15	p2_data_p_b[15]
2	P2_DATA_P10	p2_data_p_b[10]	18	P2_DATA_N15	p2_data_n_b[15]
3	P2_DATA_N10	p2_data_n_b[10]	19	GND	-
4	GND	-	20	P2_DATA_P16	p2_data_p_b[16]
5	P2_DATA_P11	p2_data_p_b[11]	21	P2_DATA_N16	p2_data_n_b[16]
6	P2_DATA_N11	p2_data_n_b[11]	22	GND	-
7	GND	-	23	P2_DATA_P17	p2_data_p_b[17]
8	P2_DATA_P12	p2_data_p_b[12]	24	P2_DATA_N17	p2_data_n_b[17]
9	P2_DATA_N12	p2_data_n_b[12]	25	GND	-
10	GND	-	26	P2_DATA_P18	p2_data_p_b[18]
11	P2_DATA_P13	p2_data_p_b[13]	27	P2_DATA_N18	p2_data_n_b[18]
12	P2_DATA_N13	p2_data_n_b[13]	28	GND	-
13	GND	-	29	P2_DATA_P19	p2_data_p_b[19]
14	P2_DATA_P14	p2_data_p_b[14]	30	P2_DATA_N19	p2_data_n_b[19]
15	P2_DATA_N14	p2_data_n_b[14]	31	GND	-
16	GND	-	32	-	-

3.5 GTP Connectors

3.5.1 GTP1

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	11	GTP1_TX_N	sata0_tx_n_o
2	-	-	12	-	-
3	-	-	13	GND	-
4	-	-	14	GND	-
5	-	-	15	GTP1_RX_N	sata0_rx_n_i
6	-	-	16	-	-
7	GND	-	17	GTP1_RX_P	sata0_rx_p_i
8	GND	-	18	-	-
9	GTP1_TX_P	sata0_tx_p_o	19	GND	-
10	-	-	20	-	-

3.5.2 GTP2

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	11	GTP2_TX_N	sata1_tx_n_o
2	-	-	12	-	-
3	-	-	13	GND	-
4	-	-	14	GND	-
5	-	-	15	GTP2_RX_N	sata1_rx_n_i
6	-	-	16	-	-
7	GND	-	17	GTP2_RX_P	sata1_rx_p_i
8	GND	-	18	-	-
9	GTP2_TX_P	sata1_tx_p_o	19	GND	-
10	-	-	20	-	-

3.6 SFP Connector, LEDs and Pushbutton

3.6.1 SFP

Pin	Signal	UCF	Pin	Signal	UCF
1	GND	-	11	GND	-
2	WR_TXFAULT	wr_txfault_i	12	SFPRX_123_N	sfprx_123_n_i
3	WR_TXDISABLE	wr_txdisable_o	13	SFPRX_123_P	sfprx_123_p_i
4	WR_MODDEF2	wr_moddef2_b	14	GND	-
5	WR_MODDEF1	wr_moddef1_o	15	3V3	-
6	WR_MODDEF0	wr_moddef0_i	16	3V3	-
7	WR_RATESELECT	wr_rateselect_o	17	GND	-
8	WR_LOS	wr_los_i	18	SFPTX_123_P	sfptx_123_p_o
9	GND	-	19	SFPTX_123_N	sfptx_123_n_o
10	GND	-	20	GND	-

3.6.2 Pushbutton and Frontpanel-LEDs

The Pushbutton is active low. The associated UCF net is *pushbutton_i*. The Frontpanel-LEDs are connected to the UCF nets *fp_ledn_o(7..0)*. For detailed connection for the LEDs one should consult the SVEC schematic.

4 Appendices

4.1 Technical Data

S FPGA

Manufacturer	Xilinx
Family	Spartan6
Type	XC6SLX9
Package	FTG256C
Speed	-2
User IOs	186

A FPGA

Manufacturer	Xilinx
Family	Spartan6
Type	XC6SLX150T
Package	FGG900
Speed	-3
User IOs	540

Memory

Type	512MB DDR3-SDRAM (667MHz)
Speed Grade	1333(MT/s)
Configuration	128 Meg x 16 bit x 8 banks (2 chips parallel / 32 bit data path)
Refresh Count	8K
Row addressing	A[13:0]
Bank addressing	BA[2:0]
Column addressing	A[9:0]
Page Size	2KB

Physical Dimensions

Width	160.00 mm
Height	233.35 mm
Weight	329 g

Environmental Specifications

Temperature range	0..+50°C (operating), -20..+75 (non-operating)
Humidity	0%..80%, non condensing

4.2 References

These references direct you to manuals and specifications that you might need to know when you attempt to program the VME64 SVEC. Most of the documents can be downloaded from the Internet. Look for the WWW servers of the chip manufacturers.

[1] http://www.ohwr.org/projects/svec
This site gives an overview of the hardware project
[2] http://www.ohwr.org/projects/svec-sw
This site gives an overview for software project for the SVEC
[3] Spartan 6 documentation
Document downloads at Xilinx
[4] CERN OHL Wiki
For a more detailed view of the license.

WWW-References

Janz Tec AG:	www.janztec.com
VITA	www.vita.com
CERN	www.cern.ch
Xilinx	www.cilinx.com
Open HW Repository	www.ohwr.org

4.3 Product History

Note that changes in the major version number are related to a PCB redesign. Though, PCB redesign need not be related to functional changes, but might have been done for manufacturing purposes only.

Version	Release Date	Name	Changes
V1.0	-	-	Product production release (as KD-FMV-SVEC0)
V2.0	08.07.2013	wbr	Product production release

4.4 Manual History

Version	Release Date	Name	Changes
V1.0	22.11.2013	ime	• Initial Version
V1.1	05.12.2013	ime	• Spelling improved
V1.2	Not released	ime	• Added